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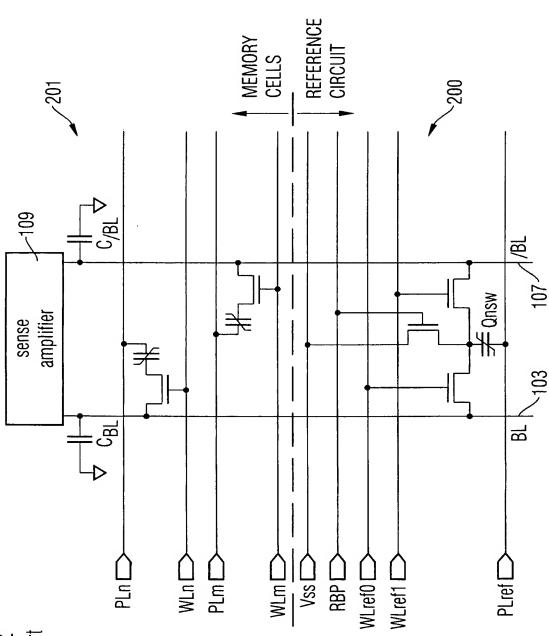
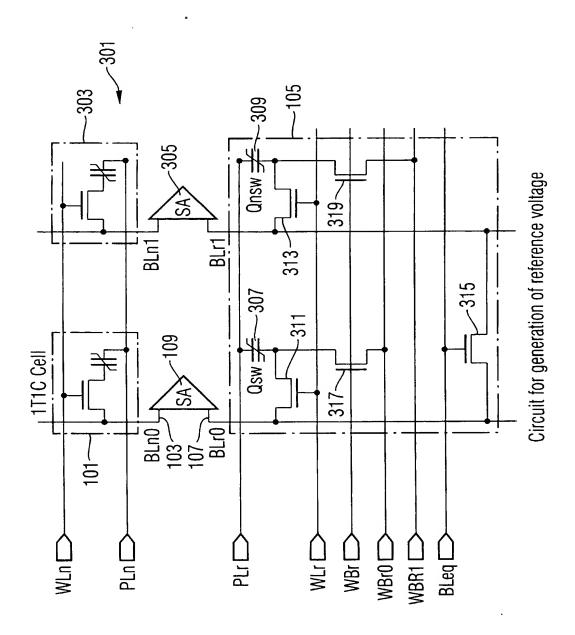


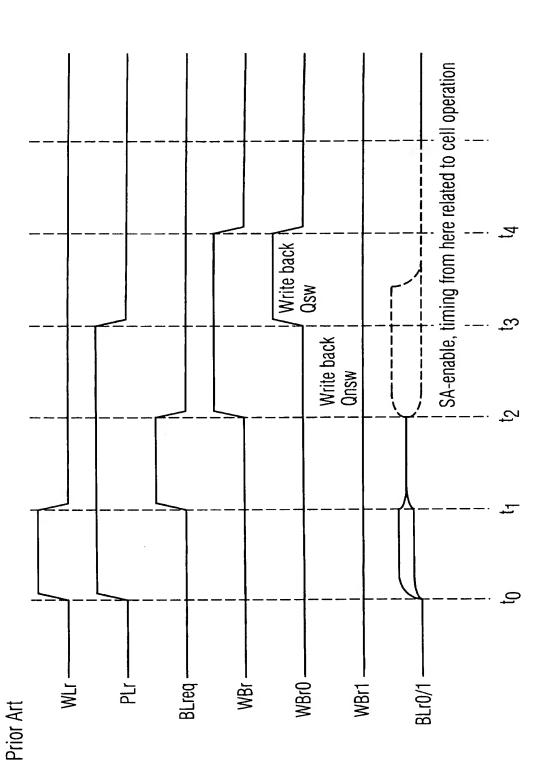
FIG 2 Prior Art

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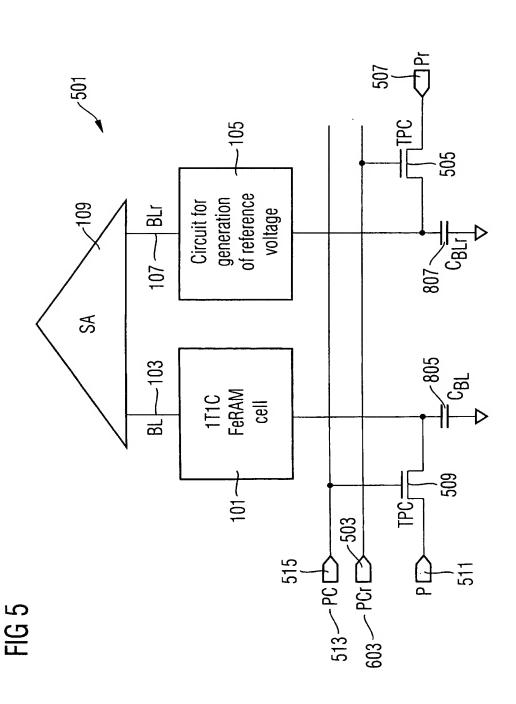
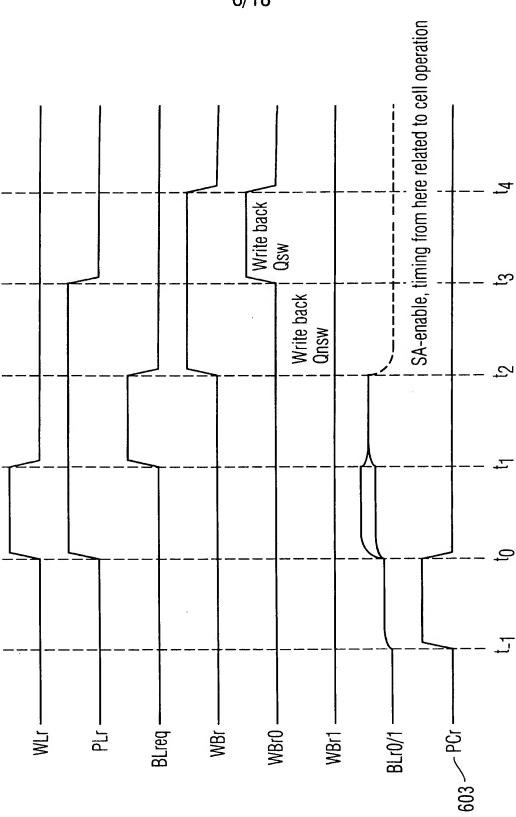
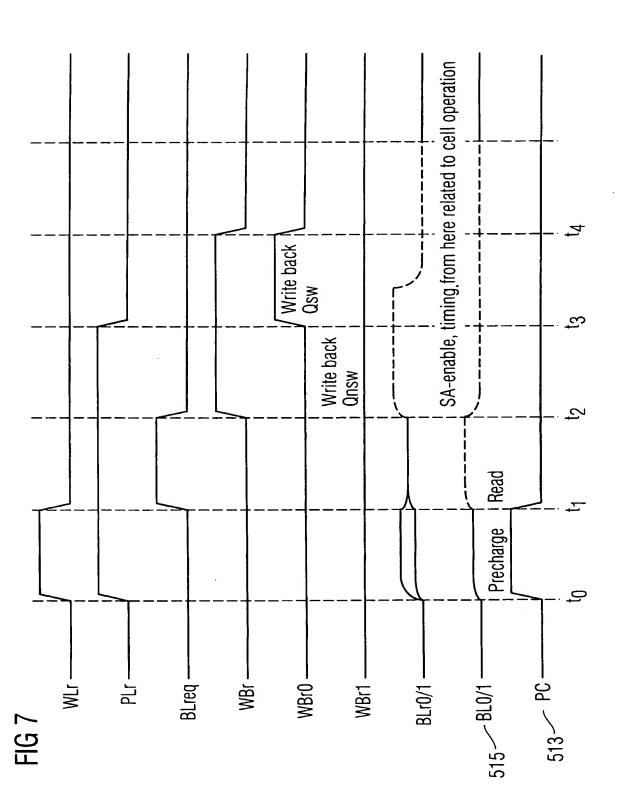


FIG 6

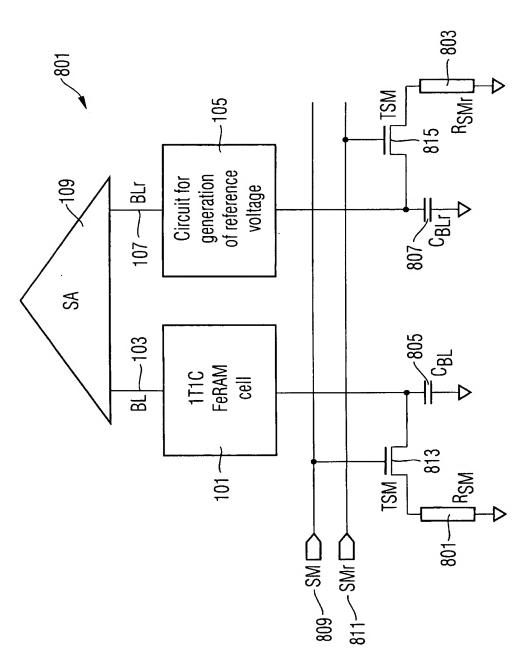




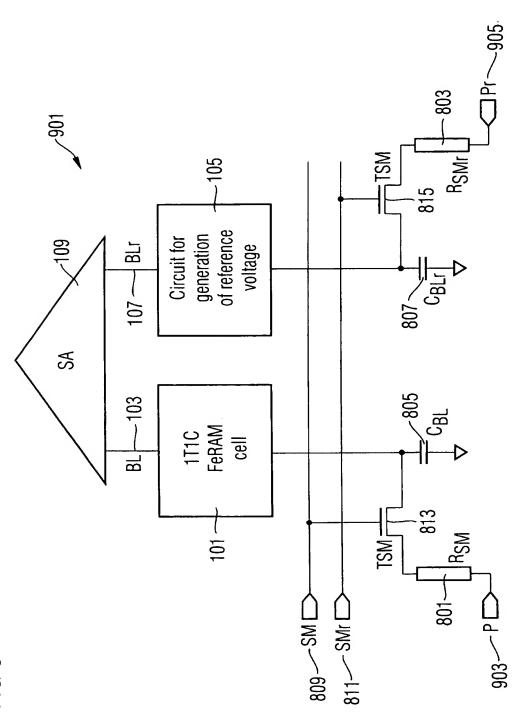
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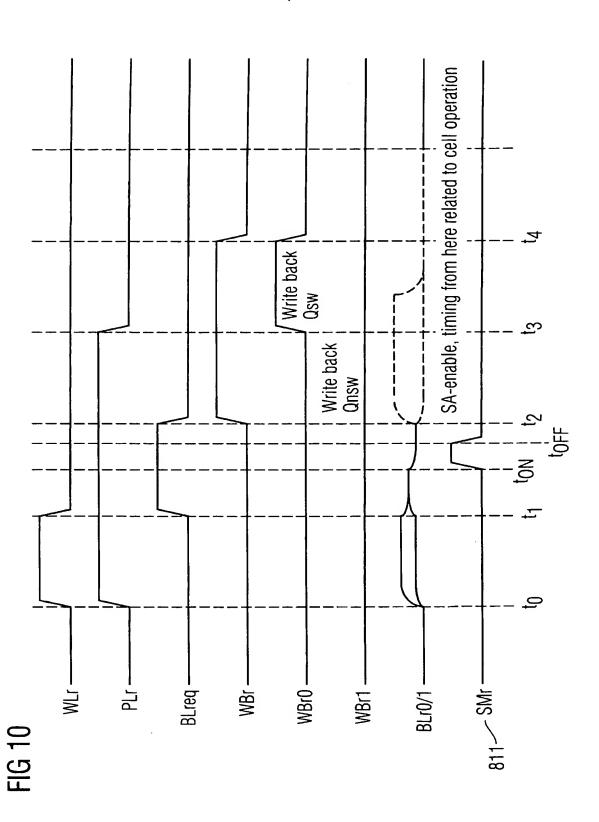


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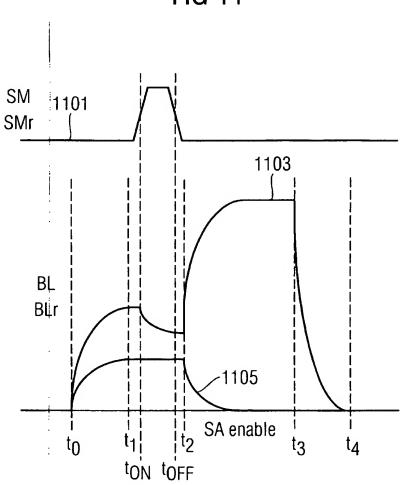
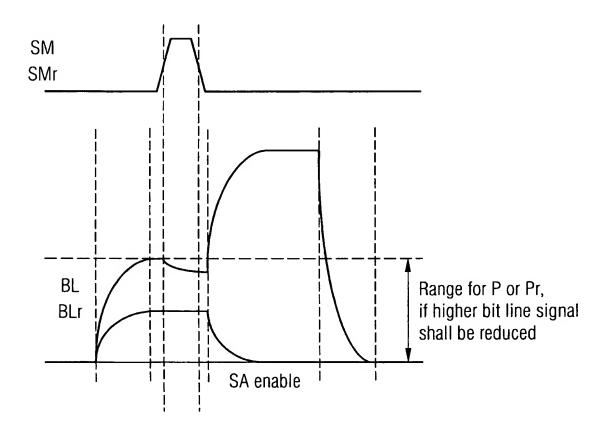


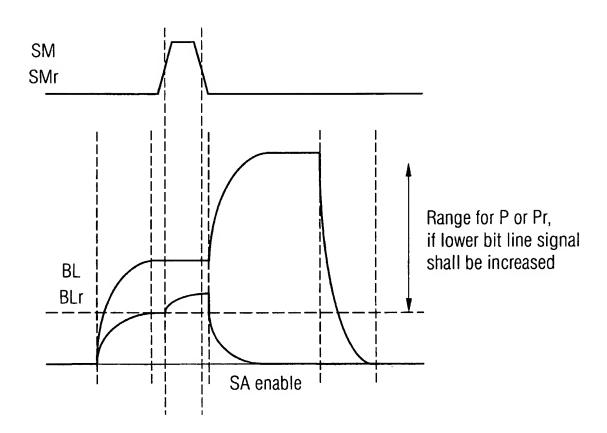
FIG 12



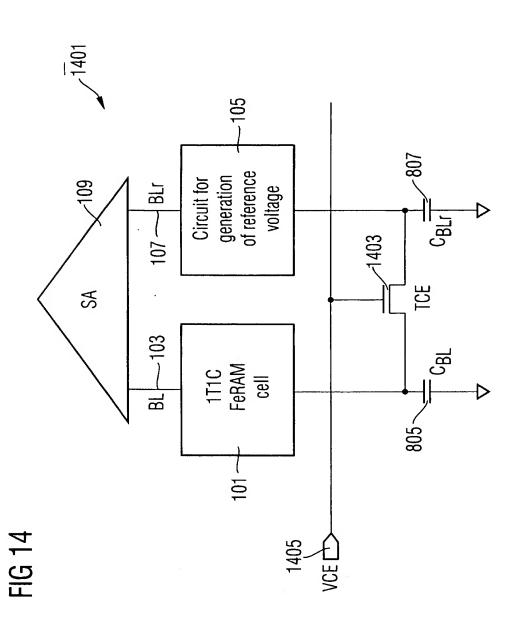
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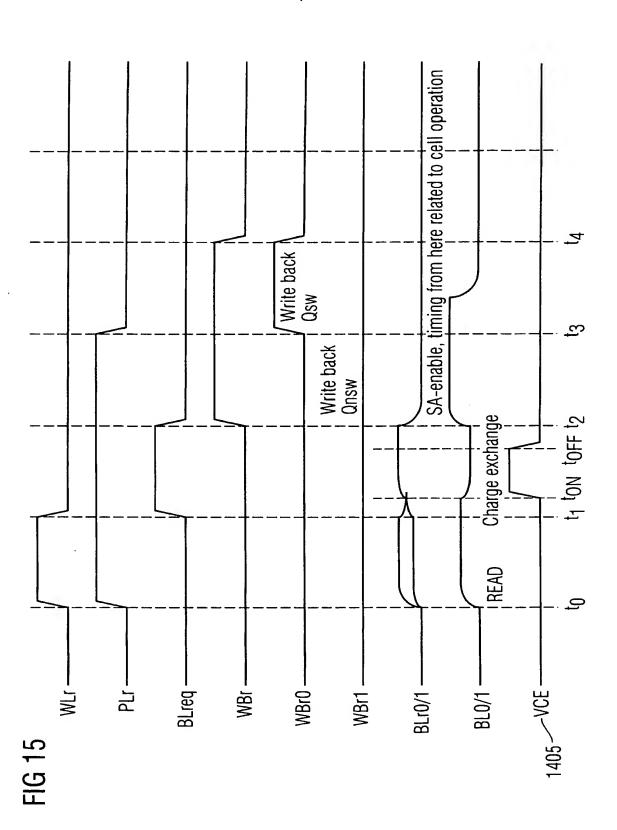
FIG 13



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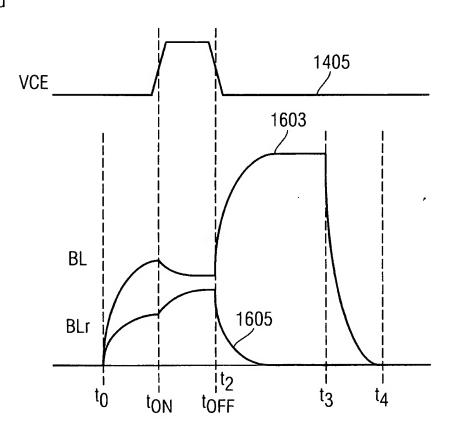
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Appln No.: 10/665,402 Pag Applicant(s): Michael Jacob et al. SIGNAL MARGIN TEST MODE FOR FERAM WITH FERROELECTRIC REFERENCE CAPACITOR

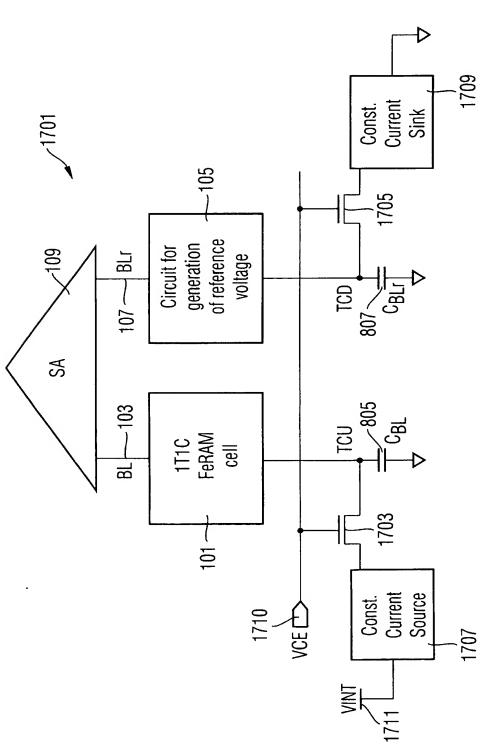
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FIG 16

read



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FIG 18

